

In re Patent Application of:
CHARLES CARPENTER
Serial No. **09/864,918**
Filing Date: **5/24/2001**
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Remarks

Applicant and the undersigned would like to thank the Examiner for his efforts in the examination of this application. Claims 1, 2, 6, 7, 11-13, 15, 19, and 20 remain in the case. Claims 1, 6, 7, 12, 13, 15, 9, and 20 were rejected under 35 USC §103(a) as being unpatentable over US Patent No. 6,321,444 to Yatsuda et al. in view of US Patent No. 6,428,650 to Chung. Claims 2 and 11 were rejected under 35 USC §103(a) as being unpatentable over US Patent No. 5,611,129 to Yoshimoto et al. in view of Chung '650 and further in view of US Patent No. 5,824,177 to Yoshihara et al.

Respectfully, the above rejections made by the Examiner can only be made with hindsight based on the guidance of the Applicant and steps presented in the claims in the case. The Examiner is asked to reconsider the rejections in view of the Declaration of Jack R. Chocola, herein attached and filed under Rule 1.132. ✓

As addressed in the Chocola Declaration, Yatsuda '444 teaches a process of making a flip-chip SAW device including the steps of forming a material having a first and second surface and a cavity with a recess to receive a lid, and sealing the lid in the recess over the inserted SAW die. Chung '650 teaches an assembly process for a plurality of optical devices and separating a wafer into individual optical devices. The Examiner rejects claims 1,6,7,12,13,15,19 and 20 contending that it would be obvious at the time of invention for a person having ordinary skill in the art to modify the process of

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fabricating a SAW device of Yatsuda '444 along with the teaching of Chung '650 for fabricating a plurality of optical devices to arrive at the teaching of the claimed invention.

As supported by the attached Declaration, one skilled in the art disagrees with the Examiner in this view. By way of example, Yatsuda '444 does not teach array processing of SAW flip-chip devices which comprise the steps of having a plurality of cavities extending into the array from the first surface, inserting a SAW die in a face down arrangement into the plurality of cavities, the plurality of cavities each have a recess for the purpose of receiving a lid, solder sealing the array and separating the array into individual SAW devices. Yatsuda '444 teaches only the assembly of a single SAW flip-chip device with a window to adjust the characteristics of the SAW device. Yatsuda '444 does not teach nor even infer the array processing of the SAW flip-chip packages as claimed. Chung '650 teaches an assembly process for a plurality of optical devices including the step of sealing a lid over each inserted optical device using an adhesive preform or a thin layer of electrically conductive material. As presented in the Declaration of one skilled in the art, using an adhesive preform or a thin layer of electrically conductive material over each optical device results in a non-hermetically sealed structure. While the sealing of devices using adhesive preforms, molded epoxy, polymer or plastic as taught by Chung (col.5 lines 10-13) may provide resistance to the passage of water into the device but will not prevent water from entering the package. Such processes are not considered as "hermetically sealing" by those skilled in the art.

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Similarly, the sealing of a metal lid with a thin layer of electrically conductive material, as taught by Chung '650 (col. 5 lines 31- 47) would provide electrostatic and/or electromagnetic shielding and resistance to the passage of moisture to within the package. To one of skill in the art, it is not considered as hermetically sealing. Specifically, Chung '650 is not directed to nor does it suggest the assembly process of an array of hermetically sealed small dimension flip-chip SAW devices. One of skill in the art relying on Chung '650 would not be aware of the challenging task of accomplishing a technique of externally fixturing the soldered lids onto an array of very small dimensioned cavities holding the flip-chip SAW die. The small dimensions of the lids associated with flip-chip SAW devices and the limited clearance between packages on the array make it difficult to maintain integrity between the external fixture and the array during solder reflow. The problem of solder bridging between the lids is prevalent. Further, it would appear that Chung '650 teaches away from solder sealing to achieve hermetically sealed device stating that true hermetically sealed packages are very expensive to fabricate (col. 1 lines 65 – 67). The claimed invention provides the teaching of forming a recess in the cavity such that the walls of the recess contain the lids during handling and prevent solder from bridging between the lids during solder reflow of the array. Neither Yatsuda '444 nor Chung '650 suggest or infer this teaching. One skilled in the art would not find the claimed invention obvious based on the teachings of Yatsuda '444 and Chung '650. As such, it would appear that the steps

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presented in independent claims 1 and 19 could only result from the Applicant's teachings and not from a combination of the cited references as the Examiner would suggest. While often difficult, one must imagine what one skilled in the art would have thought to be obvious without a reading of the Applicant's teachings. Otherwise, it is only through hindsight that such a conclusion can be reached.

The Examiner rejects Claims 2 and 11 as being unpatentable over Yoshimoto '129 in view of Chung '650 and further in view of Yoshihara '177. Yoshimoto '129 teaches a method of assembling bulk wave piezoelectric oscillators in an array of resinous packages. Since the package is resinous, it is well known to those of skill in the art that it would not provide a hermetic seal. Yoshimoto '129 teaches assembly of bulk wave devices and not surface acoustic wave devices mounted in a flip-chip arrangement in an array. As above discussed, Chung '650 teaches an assembly process of optical devices, which includes the step of sealing the optical devices using adhesive preforms or a thin layer of electrically conductive layer, which results in a non-hermetically sealed device. Neither Chung '650 nor Yoshimoto '129 teach a method of manufacturing an array of hermetically sealed surface acoustic wave devices, with the method comprising the steps of forming a recess within the cavity of the array, inserting and attaching a SAW die face down (in a flip-chip arrangement), and solder sealing a metal lid in the recess over the inserted SAW die to hermetically seal the SAW die within the cavity. To one skilled in the art, these steps clearly distinguish over and are

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not obvious from the teachings of known prior art and in particular over Yoshihara '177 and Chung '650. As further supported by the Declaration of Jack R. Chocola, one skilled in the art would not look to the teachings of Yoshihara '177 and Chung '650 to arrive at the claimed inventions as identified in Claims 2 and 11.

Commercial success of an invention must not be ignored, especially when it is attributable to the merits of the claimed invention. Such is persuasive evidence of nonobviousness. As indicated in the attached Declaration, the method for manufacturing an array of hermetically sealed SAW devices as presented in the claims pending in this application have resulted in commercial success of resulting product delivered by Sawtek, Inc. to its customers. As indicated, the array process of flip-chip devices as taught in by this patent application has been successfully applied to the high volume production for a number of SAW filters for application in mobile telecommunication systems. At least a million of such devices being produced in the last couple of years with a desirable yield that reflects the "robustness" and value of the claimed process.

Applicant respectfully submits that the above arguments are sufficient to overcome the rejections made in this case, and this application is now in a condition for allowance. Passage to issue is respectfully solicited. The Applicant and the undersigned would like to again thank the Examiner for his efforts in the examination of this application and for reconsideration of the claims as amended in light of the



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arguments presented. If the further prosecution of the application can be facilitated through telephone interview between the Examiner and the undersigned, the Examiner is requested to telephone the undersigned at the Examiner's convenience.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that the foregoing is being deposited with the United States Postal Service as first class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, this 23rd day of September, 2004.

Edward Bradley